ABSTRACT

A pipelined, simultaneous and redundantly threaded ("SRT") processor comprising, among other components, load/store units configured to perform load and store operations to or from data locations such as a data cache and data registers and a cycle counter configured to keep a running count of processor clock cycles. The processor is configured to detect transient faults during program execution by executing instructions in at least two redundant copies of a program thread and wherein false errors caused by incorrectly replicating cycle count values in the redundant program threads are avoided by implementing a cycle count queue for storing the actual values fetched by read cycle count instructions in the first program thread. The load/store units then access the cycle count queue and not the cycle counter to fetch cycle count values in response to read cycle count instructions in the second program thread.